

Development of CoRDIA: a detector for diffraction-limited SRs and CW FELs

A. Marras^{1,2}, A. Klyuev^{1,2}, T. Laurus^{1,2}, D. Pennicard^{1,2}, U. Trunk^{1,2},
C.B. Wunderer^{1,2}, T. Hemperek³, T. Kamilaris³, H. Krueger³, T. Wang³
and H. Graafsma^{1,2,4}

1) *Deutsches Elektronen-Synchrotron (DESY), Hamburg, Germany*

2) *Center for Free Electron Laser Science (CFEL), Hamburg, Germany*

3) *University of Bonn, Bonn, Germany*

4) *Mid Sweden University, Sundsvall, Sweden*

CoRDIA



SRs becoming diffraction-limited



expect brilliance increment $O(2)$
~continuous frame rate

high-brill. FELs considering CW operation

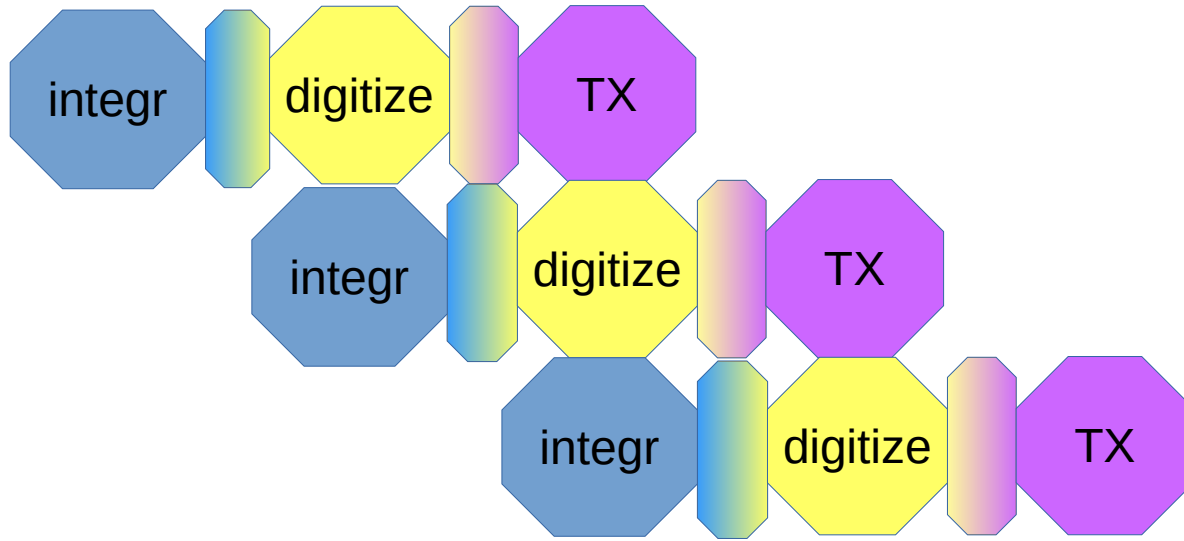


expect ~continuous operation in
the 100kHz + range, no time gaps
exp. pulse intensity ~ today

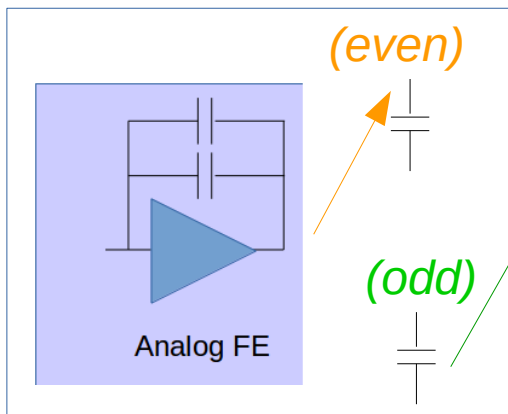
common need emerging

our goals

- > 100 kHz, continuous
- 100 μm pixel size
- minimal dead area
- charge integrating
- 1-photon sens. 12 keV
- 10k ph/pix/img (or more)
- compatible with HZ & internal-ampl. sensors



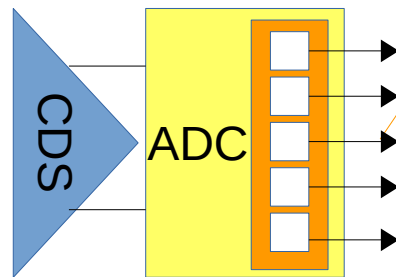
CWR scheme using pipelined signal-process chain



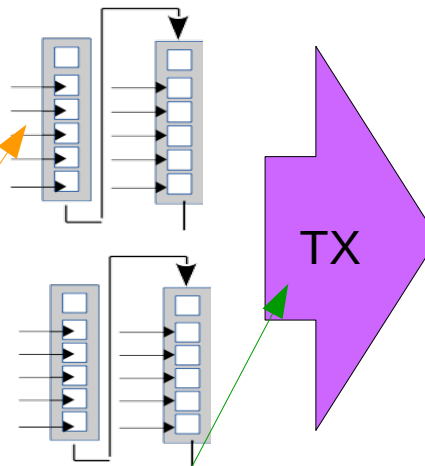
16x integrating FE

(even)

(odd)



shared CDS/ADC

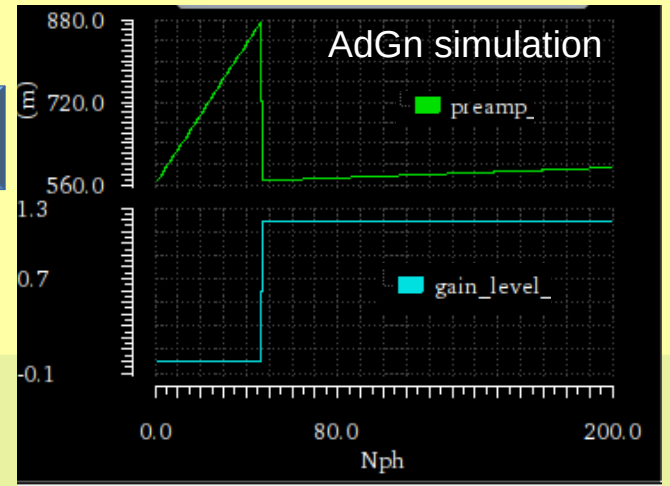
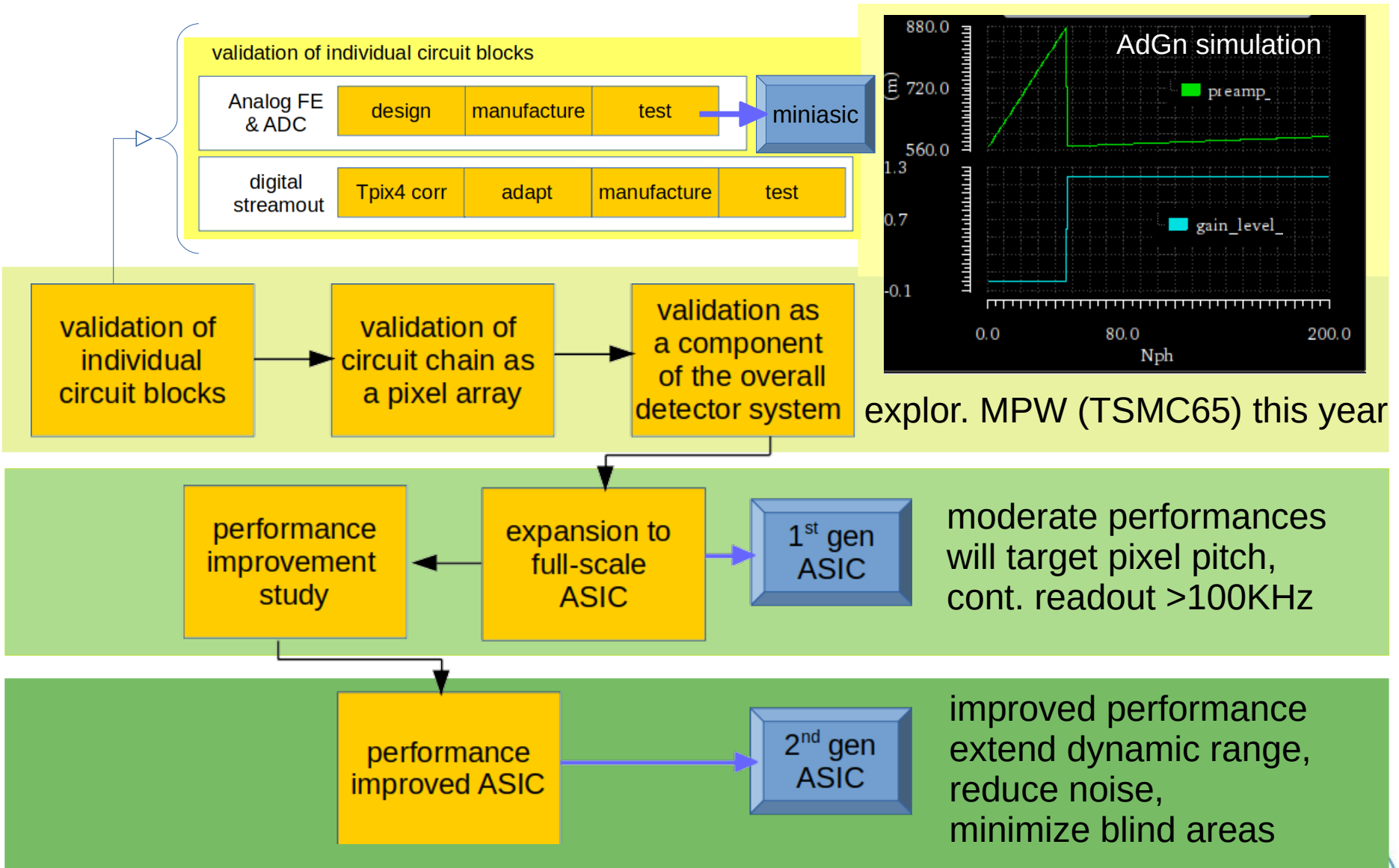


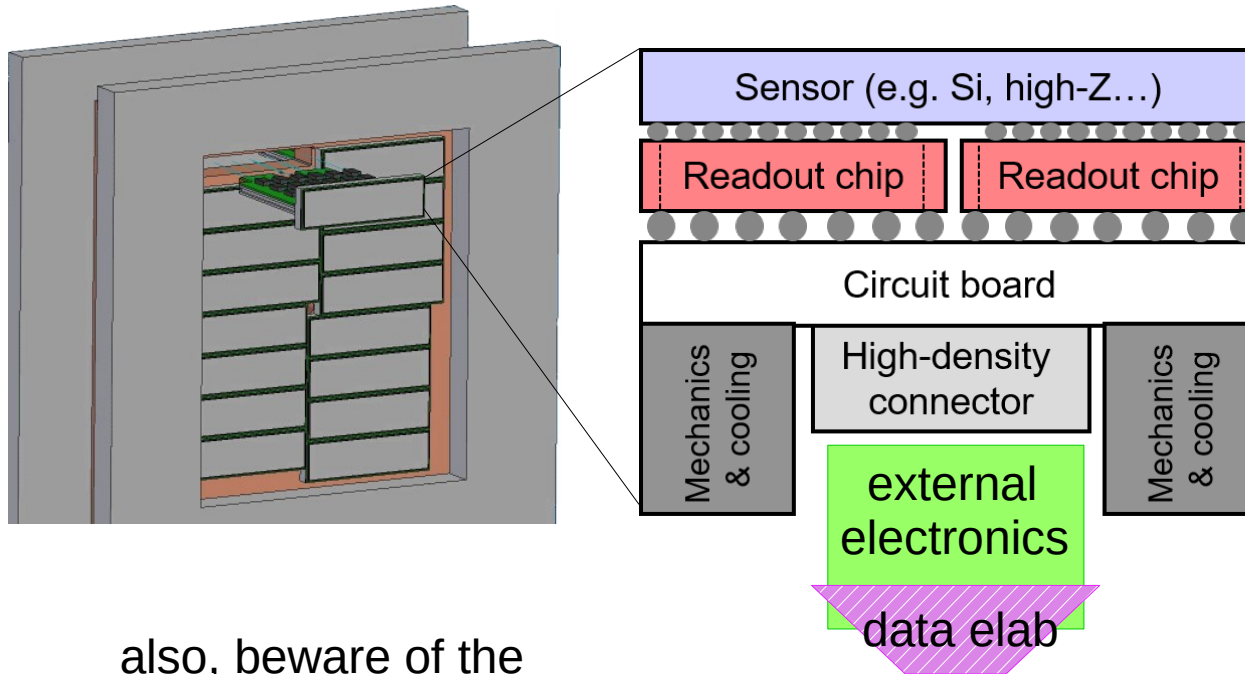
GWT

AdGn FE adapt. from AGIPD

on-chip ADC developed by Bonn University

adopt. Timepix4 GWT developed by Nikhef





compatibility with e-collecting sensors:

- n-on-p Si (~12keV)
- high-Z (hard X-rays)
- sensors with built-in amplification (soft X-rays)

plan to use TSVs to minimize dead/blind space between modules

also, beware of the **DataApocalypse**

$$1\text{Mpix} \times 14\text{bit/pix} \times 100\text{kframe/s} = 1.4\text{Tb/s} = 175\text{GByte/s}$$

or worse, as:

larger array desirable

encoding, redundancy

>100kframe/s

we plan to address the issue:

On Silicon

- on-chip digitization through parallel ADCs
- high speed drivers

Out-of-Silicon:

- Serialization on high-perform. FPGA
- high-speed optical links

data reduct./compress.:
(under consideration)

- preproc. hardware to reduce data volume