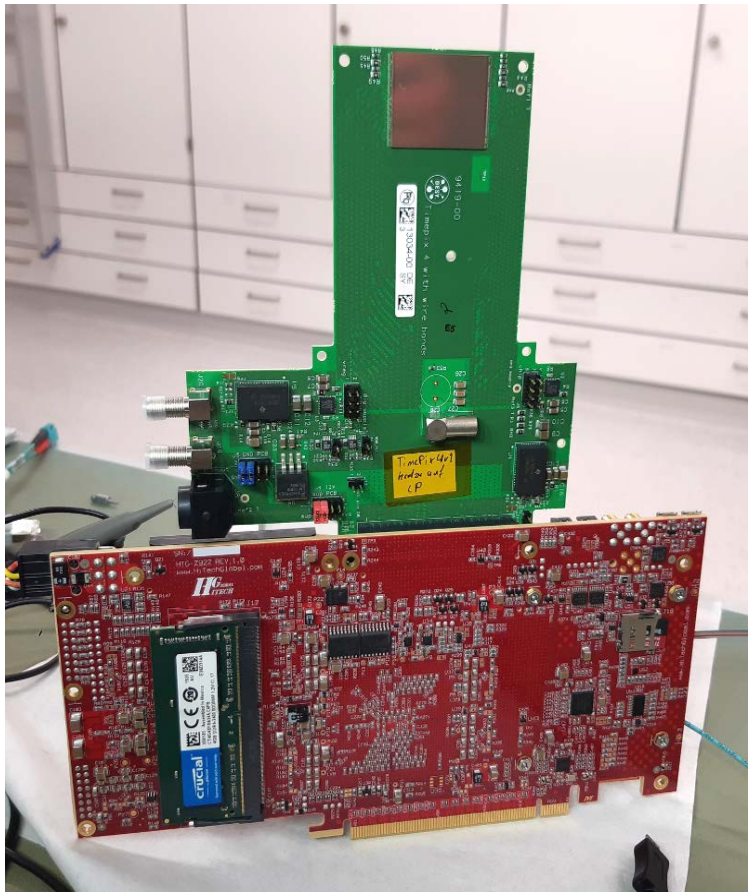
TimePix4, a versatile timestamping pixel detector



Jonathan Correa, David Pennicard, Sabine Lange, Sergej Smoljanin, Sergei Fridman, Vahagn Vardanyan, and Heinz Graafsma

DESY Photon Science Detector Group (FS-DS)

IFDEPS virtual Thursdays, 08.04.2021

HELMHOLTZ | ASSOCIATION

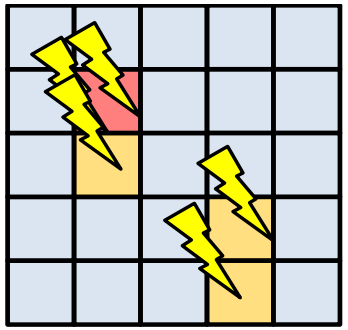
DESY

Timepix4 readout chip – key features

> Developed by CERN on behalf of Medipix4 collaboration

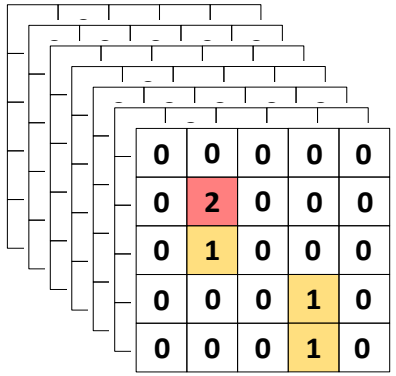
Photon counting mode

Detector



55 µm pixels

Frame readout

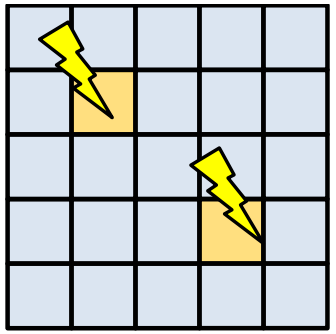


Improves on Medipix3 (single threshold):

- 40 kHz frame rate CRW (8 bit depth)
- ~ 5x10^6 counts/pixel/s

Event-by-event mode

Detector



55 µm pixels

Data packets

Pixel (1,1)
Energy ~15 keV
Time 525 ns

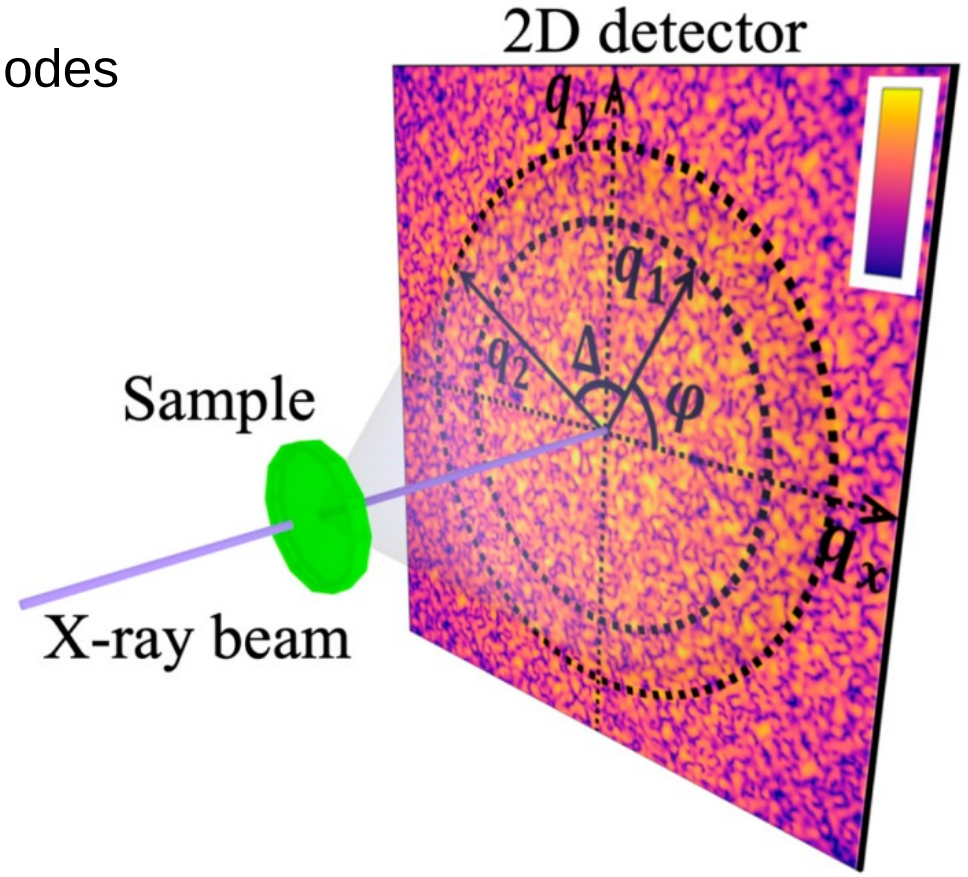
Pixel (3,3)
Energy ~10 keV
Time 765 ns

Improves on Timepix3:

- Event rate: ~10^9 events/s in 512 x 450 pixel chip
- Up to 150 ps RMS time resolution (sensor dependent)
- ~ 2 keV energy resolution

Example application – coherence beamlines at DLSRs

- Can flexibly switch between photon counting and event modes
- **Photon counting mode for scanning techniques**
  - Scanning nano-SAXS, holography…
- **Event mode for extreme time resolution**
  - Can identify which bunch each photon comes from
  - XPCS and other correlation techniques
    - Sub-microsecond correlation times

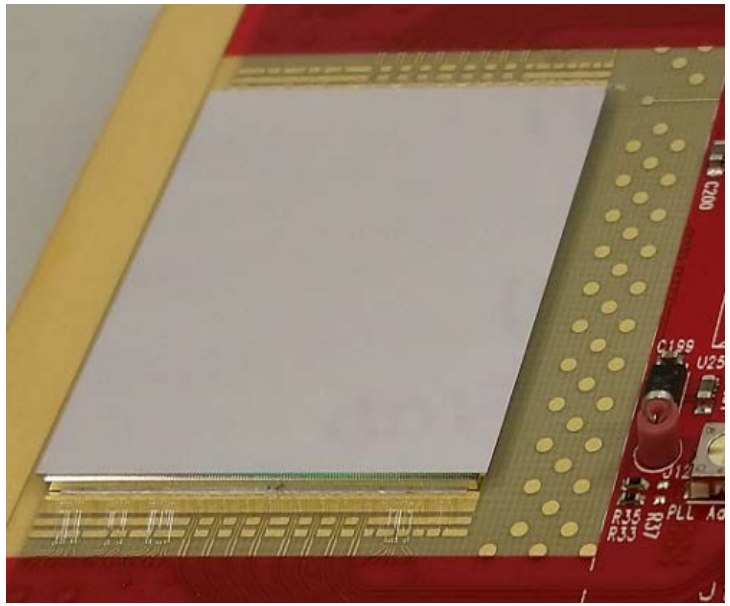


Also pump-probe experiments, photoionisation experiments, nuclear resonant scattering…

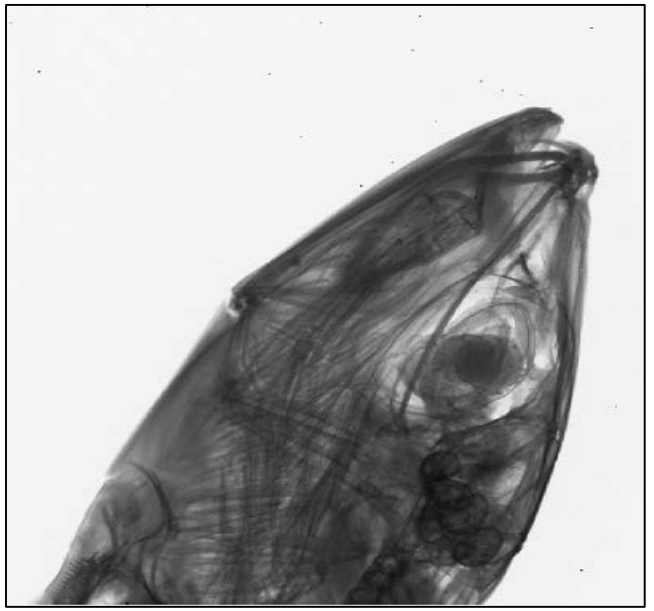
I. Zaluzhnyy et al, Materials 12(21), 3464, 2019.
doi: 10.3390/ma12213464

Status of chip

- Chip tested by CERN – most specifications reached
- Bug prevents full-speed readout under normal operating conditions
  - Bug fix found and tested with MPW
- Revised chip available later this year



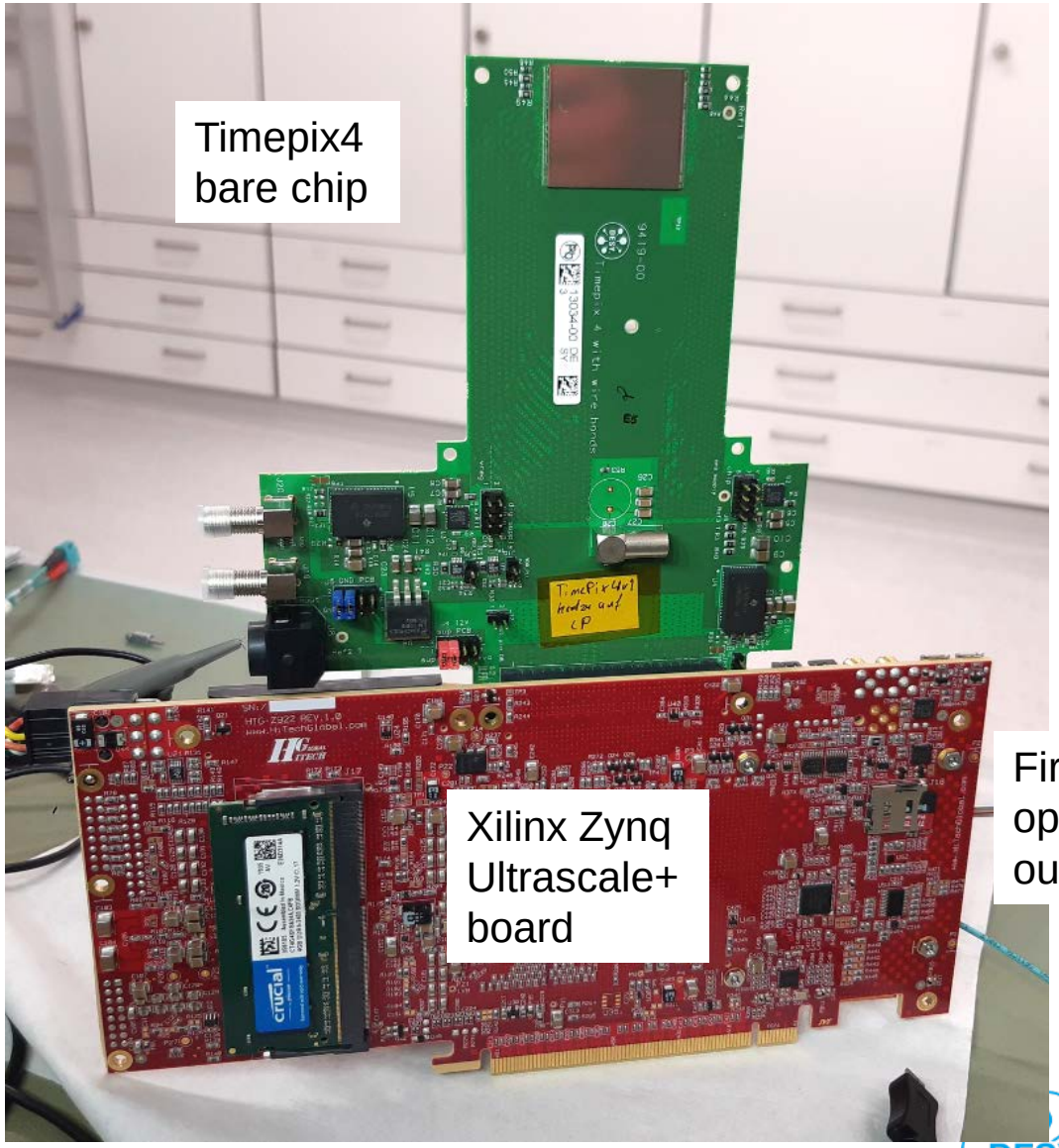
Timepix4 with Si sensor



X-ray image of fish
(thanks to Xavi Llopart)

Readout development at DESY

- Currently developing single-chip readout with Xilinx evaluation board
  - Communication with chip working
  - Challenge: Up to 160 Gbit/s bandwidth!
- Long-term plan – multi-megapixel systems using Through Silicon Vias
  - Various improvements of TSV design implemented, e.g. better landing pads and redundant inputs



> ADDITIONAL INFORMATION

Timepix series specifications

			Timepix3 (2013)	Timepix4 (2019/20)	
Technology			IBM 130 nm – 8 metal	TSMC 65 nm – 10 metal	
Pixel size			55 x 55 µm	55 x 55 µm	
Pixel arrangement			3-side buttable 256 x 256	4-side buttable (TSV) 512 x 448	**3.5 x**
Sensitive area			1.98 cm^2	6.94 cm^2	
Readout modes	**Data driven (tracking)**	**Mode**	ToT and TOA		
		Event packet	48-bit	64-bit	
		Max rate	< 43 Mhits/cm^2/s	357.6 Mhits/cm^2/s	**8 x**
		Pix rate equiv.	1.3 kHz/pix average	10.8 kHz/pix average	
	Frame Based (imaging)	**Mode**	Count: 10 bit + iToT	Count: 8 or 16 bit CRW	
		Frame	Zero suppressed (with pix addr)	Full frame (no pix addr)	
		Max count rate	82 Ghits/cm^2/s	~ 800 Ghits/cm^2/s	**10 x**
		Max frame rate	N/A (worst case: 0.8ms readout)	80 kHz CRW	
TOT energy resolution			< 2 keV	< 1 keV	**2 x**
Time resolution			1.56 ns	~ 200 ps	**8 x**
Readout bandwidth			≤ 5.12 Gbps (8 x 640 Mbps)	≤163.8 Gbps (16 x 10.2 Gbps)	**32 x**
Target minimum threshold			< 500 e^-	< 500 e^-	

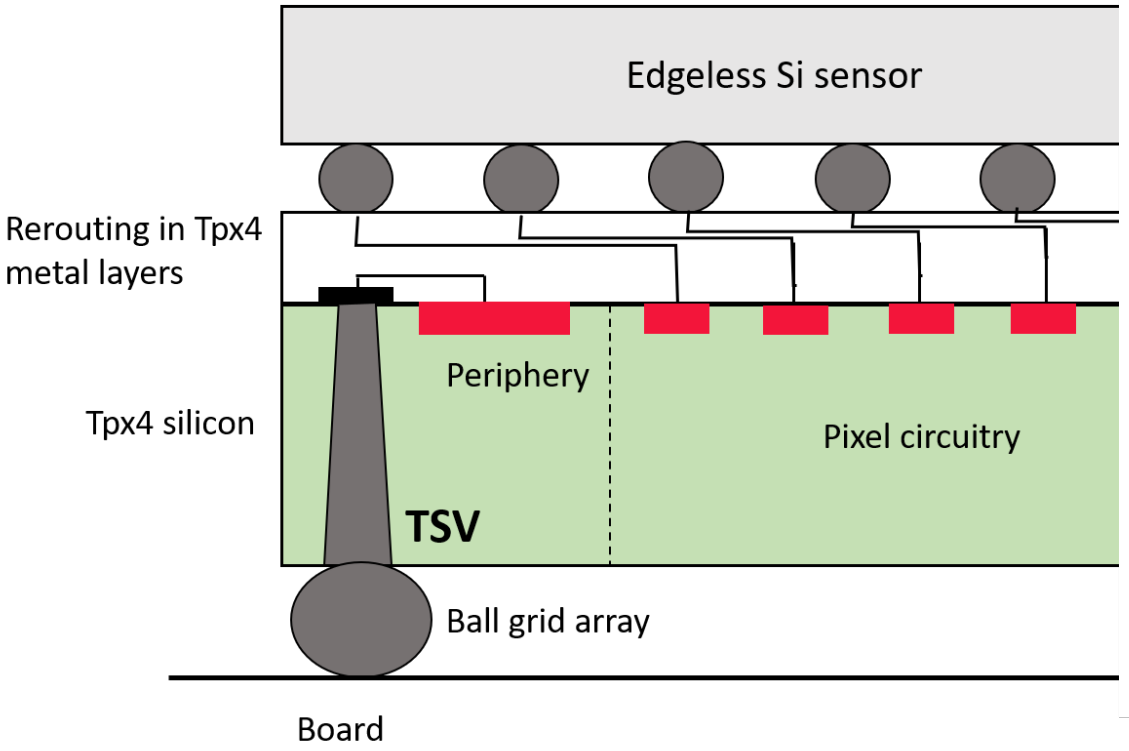
Notes:

Event rate and frame rate shown here assume readout at maximum speed, but on slide 2 I assume half readout rate for a conservative estimate.

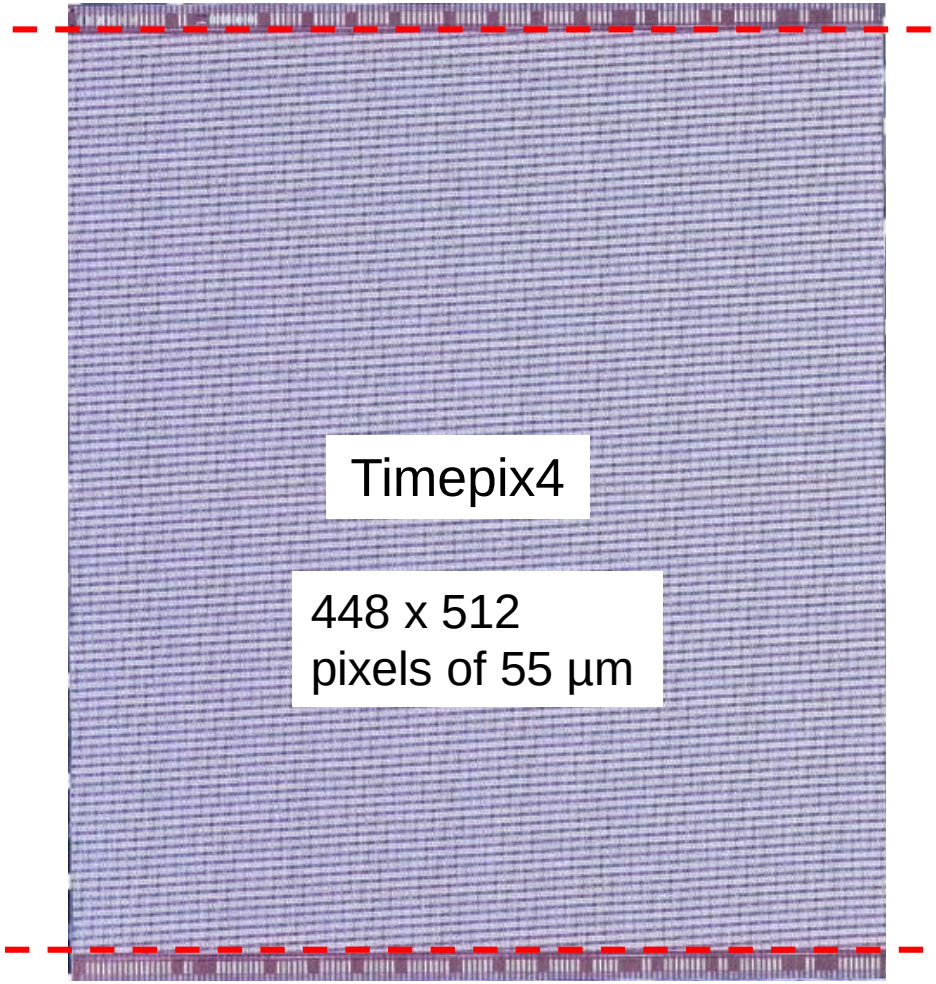
Frame mode count rates give the theoretical maximum. With random photon hits, 10% nonlinearity will occur at 10% of this rate. On slide 2 I assume we can measure ½ the theoretical maximum after count rate correction.

Improved 4-side butting with Through-Silicon Vias

- With TSVs, full chip surface is covered with pixels
  - Rerouting in metal layers creates space for periphery
- Improved TSV landing pads, redundant inputs, extra power TSV connections in centre of chip



Wire bond pads can be diced off



Expected applications around DESY